PWM-BASED DC-DC CONVERTER WITH ASSURED DEAD TIME CONTROL EXHIBITING NO SHOOT-THROUGH CURRENT AND INDEPENDENT OF TYPE OF FET USED

CROSS-REFERENCE TO RELATED APPLICATION

[001] The present application claims the benefit of co-pending U.S. Patent Application Serial No. 60/437,180 filed December 31, 2002, by N. Dequina et al, entitled: "Assured Dead Time Control Exhibiting No Shoot-Through Current and Independent of Type of FET Used," assigned to the assignee of the present application and the disclosure of which is incorporated herein.

FIELD OF THE INVENTION

[002] The present invention relates in general to DC power supply circuits and components therefor, and is particularly directed to a new and improved pulse width modulator (PWM)-based DC-DC converter circuit, that is configured to maintain a fixed dead time that exhibits no shoot-through current and is independent of the type of switching FET used.

BACKGROUND OF THE INVENTION

[003] Electrical power for an integrated circuit (IC) is typically supplied by one or more direct current (battery) power sources, such as a pulse width modulation (PWM)-based, DC-DC converter. As diagrammatically illustrated in Figure 1, this type of converter contains a PWM signal generator 1 that supplies a synchronous PWM signal to a switching circuit driver 2. Such a PWM-based converter architecture is ideally intended to deliver constant energy to an output node regardless of the input voltage. To this end, the switching circuit driver 2 controls the on-time and off-time of a pair of electronic power switching devices 3 and 4 (typically external NFETs) connected between power supply rails Vin and ground (GND). A common or PHASE node 5 between the two FETs is coupled through an inductor 6 to a load reservoir capacitor 7, with the connection 8 between inductor 6 and capacitor 7 serving as an output node from which a desired (regulated) DC output voltage is applied to load 9.

[004] The circuit of Figure 1 typically operates in the manner shown in the set of timing diagrams of Figure 2. In particular, in response to a positive-going transition 201 in a PWM waveform 200, the FET driver 2 turns off the LGATE drive to the lower FET 4. In response to the LGATE voltage 210 dropping to a prescribed threshold detection value 211 (e.g., 1.5 V), the driver control circuitry 2 applies a UGATE turn on voltage 220 which exhibits a positive excursion 221 to

the gate drive input of the upper FET 3. The voltage at the PHASE node represented by signal trace 230 substantially follows the upper gate voltage signal and is monitored to control the turn-on of the LFET 4.

[005] In particular, in response to a negative-going transition 202 in the PWM signal 200, the UGATE signal undergoes a high to low transition 222, turning off the UFET 3. Then, in response to the associated excursion 232 in the PHASE node voltage 230 dropping to a predetermined threshold detection value 233, the LGATE voltage is transitioned high, as shown by the positive-going excursion 212 of the LGATE signal 210, turning on the LFET 4. Figure 2 also shows the application of a tristate or power-on reset signal 240 having rising edge 241 to turn off the lower gate drive signal at 213 and falling edge 242 to turn on the lower gate signal at 214.

[006] In the course of terminating the on-time of each FET switch, it is desirable to provide a time interval during which both controlled switches (UFET 3 and LFET 4) are guaranteed to be off. This time interval, known as 'dead time', allows for the resetting of magnetic circuit components within the power supply. Namely, modulation of the PWM generator's duty cycle is limited, in order to insure that there always exists a dead time period. This also serves to prevent efficiency degradation, which occurs when both the upper and lower FETs intermittently conduct during a common time interval. This unwanted intermittent conduction problem

results from insufficient dead time before the other FET begins conduction. Among factors that contribute to this phenomenon are the type of FET being used and board parasitic layout.

SUMMARY OF THE INVENTION

[007] In accordance with the present invention the above assured 'dead time' objective is successfully addressed by a switching mode-based DC-DC converter signal processing architecture, which is configured to guarantee that each of the upper and lower FETs of a switched FET pair is completely turned off before its complementary device (the other FET of the switched pair) begins conduction, irrespective of the type of FET being used. As will be described, the invention employs prescribed voltage threshold and time-out (delay) detectors that are selectively coupled to monitor LOWER GATE, UPPER GATE and PHASE nodes of the switching FETs. These monitored values are processed in a set of combinational logic to generate control signals for establishing drive signals that are used to turn the upper and lower FETS on and off.

[008] To this end, subsequent to a prescribed blanking delay following a low-to-high transition in the PWM signal, the lower FET's gate drive signal is caused to transition from high-to-low, turning the LFET off. Using this high-to-low transition of the LFET signal as detected by an LGATE detector as a reference, the PHASE node voltage is monitored by phase node detectors for

one of a set of predetermined conditions in order to determine when to turn on the UFET. The invention addresses three separate cases that may initiate turn on of the UFET by way of the UGATE signal. For each action, there is a built-in precedent blanking delay following detection of the high-to-low transition of the LGATE signal.

[009] A first case corresponds to the polarity of the voltage at the PHASE node going negative after the LGATE node transitions from high-to-low. In response to the LGATE voltage going low, the voltage at the PHASE node is monitored to determine whether it has reached a prescribed negative polarity voltage (e.g., -0.4 V). In particular, following a blanking delay, if the phase voltage at the PHASE node drops below the -0.4 V threshold, combinational logic triggers a low-to-high to transition on the UGATE, which causes the phase node voltage to go high.

[010] The second case is associated with a reverse current condition, and corresponds to the polarity of the voltage at the PHASE node going positive subsequent to the LGATE node transitioning from high-to-low. For this purpose, if Case I is not observed, namely, if the -0.4 V threshold is not reached following the high-to-low transition of the LGATE voltage, combinational logic looks to see whether a prescribed positive threshold (e.g., +0.6 V) has been reached. If so, the combinational logic will trigger a low-to-high

transition of the UGATE signal, which causes the phase node voltage to go high.

[011] The third case associated with a no load condition, corresponds to the elapse of a prescribed time-out without either of the positive and negative polarity thresholds having been reached at the phase node. Namely, if neither the -0.4 V and +0.6 V thresholds is observed at the phase node within a prescribed time out window after the high-to-low transition in the LGATE signal, the combination logic triggers a low-to-high transition of the UGATE signal so that the voltage at the phase node goes high.

[012] A comparison of the LGATE turn-off transition with the respective UGATE turn-on transitions represented by the phase node voltage traces reveals no overlap between the terminal end of the conduction interval for the LFET and the initial portion of the conduction interval for the UFET. Therefore, there is no simultaneous conduction of these two FETS between the time of turn-off of the LFET and the time of turn-on of the UFET in response to a low-to-high transition in the PWM signal.

[013] The controlled turn-off of the UFET and the subsequent turn-on of the LFET after a high-to-low transition in the PWM signal proceeds as follows. Turn-off of the UGATE drive to the UFET is initiated by a high-to-low transition in the PWM waveform. Thereafter, the PHASE node and UGATE node are monitored by associated threshold circuits within a dead time controller. Specifically, in response to the UGATE

voltage dropping to a voltage level that is a prescribed value above the phase voltage (e.g., on the order of 1.75 V above the PHASE voltage (112V)), a prescribed time out (e.g., 10 ns) is triggered, whereupon the LGATE signal is transitioned from low-to-high, turning on the LFET.

[014] Alternatively, if the level of the PHASE node voltage reaches a predetermined threshold (e.g., on the order of 0.8 V), a low-to-high transition of the LGATE voltage is initiated. As is the case for a low-to-high transition of the PWM signal, a comparison of the LGATE turn-on transition with the UGATE turn-off transition reveals that there is no overlap between the terminal end of the conduction interval for the UFET and the initial portion of the conduction interval for the LFET, so that simultaneous conduction of the two FETS between turn-off of the UFET and turn-on of the LFET cannot occur in response to a high-to-low transition in the PWM signal.

BRIEF DESCRIPTION OF THE DRAWINGS

[015] Figure 1 diagrammatically illustrates the basic architecture of a PWM-based DC-DC converter;

[016] Figures 2A-2E contain a set of timing diagrams associated with the operation of the DC-DC converter of Figure 1;

[017] Figure 3 diagrammatically illustrates a PWM-based, DC-DC converter in accordance with the present invention; and

[018] Figures 4A-4E and 5A-5D are timing diagrams associated with the operation of the DC-DC converter of Figure 3.

DETAILED DESCRIPTION

[019] Before describing in detail the PWM-based DC-DC converter circuit in accordance with the present invention, it should be observed that the invention resides primarily in a prescribed modular arrangement of conventional circuits and components therefor. In a practical implementation that facilitates their being packaged in a hardware-efficient configuration, this arrangement may be readily implemented as a field programmable gate array (FPGA), or application specific integrated circuit (ASIC) chip set. Consequently, the configuration of such arrangement of circuits and components and the manner in which they are interfaced with other electronic circuitry have, for the most part, been illustrated in the drawings by readily understandable block diagrams, which show only those specific details that are pertinent to the present invention, so as not to obscure the disclosure with details which will be readily apparent to those skilled in the art having the benefit of the description herein. Thus, the block diagram illustrations are primarily intended to show the major components of the invention in a convenient functional grouping, whereby the present invention may be more readily understood.

[020] Attention is now directed to Figure 3, wherein the architecture of a PWM-based DC-DC converter in accordance with the present invention is diagrammatically illustrated. As shown therein, an overvoltage protection (OVP) control circuit 10, to which a power on reset (POR) signal is supplied, is coupled to respective upper and lower pre-driver circuits 30 and 40, that are operative to supply gate drive signals to the upper NFET 3 and to the lower NFET 4. In addition, an overvoltage protection resistor 50 is coupled between the phase node 5 and the LGATE input to the lower NFET 4. The upper pre-driver 30 has first and second output control lines 31 and 32 coupled to the gate drives of a PFET switch 33 and an NFET switch 34, respectively. PFET switch 33 and NFET switch 34 have their source-drain paths coupled in series between an external bootstrap supply node BOOT and PHASE node 5. The common connection 35 of PFET 33 and NFET 34 is coupled as an upper gate drive UGATE to the upper NFET 3.

[021] In a complementary manner, the lower pre-driver 40 has first and second output control lines 41 and 42 coupled to the gate drive of a PFET switch 43 and an NFET switch 44, respectively. PFET switch 43 and NFET switch 44 have their source-drain paths coupled in series between a line voltage supply node LVCC and a power ground (PGND) node. The common connection 45 of PFET 43 and NFET 44 is coupled as a lower gate drive LGATE to the lower NFET 4.

[022] The control inputs to the upper pre-driver 30 are supplied by an upper level shifter 36, control for which is supplied by a set of combinational logic 60 within a dead time controller, shown surrounded by broken lines 100. Similarly, control inputs to the lower pre-driver 40 are supplied by a lower level shifter 46, control for which is also supplied by combinational logic 60 within dead time controller 100. In addition to receiving the PWM signal from an upstream PWM generator, combinational logic 60 is coupled to receive outputs of a set of voltage threshold detectors. These threshold detectors include an LGATE detector 110, which is coupled to monitor the voltage at the LGATE node 45, a +0.8 V PHASE detector 120, which is coupled to monitor the voltage at phase node 5, a -0.4 V PHASE detector 130, which is also coupled to monitor the voltage at phase node 5, a UGATE detector 140, which is coupled to monitor the voltage at the UGATE node 35, and an UP_DOWN SHIFTER 150, which is coupled to the output of the UGATE detector 140.

[023] Operation of the converter of Figure 3 may be understood by reference to the timing diagrams of Figures 4A-4E and 5A-5D. With reference to Figures 4A-4E, subsequent to a prescribed blanking delay 410-D (e.g., on the order of 7 ns) following a first low-to-high transition 401 of the PWM signal 400, the lower FET's gate drive signal 410 applied to the LGATE node 45 is caused to transition from high to low, as shown by excursion 411, turning the LFET 4 off. Using this high-to-low transition 411 of the LFET signal as detected by

LGATE detector 110 as a reference, the PHASE node voltage (PHASE) is then monitored by phase node detectors 120 and 130 for the occurrence of one of a set of predetermined conditions in order to determine when to turn on the UFET 3. The invention addresses three separate cases that may initiate turn on of UFET 3 by way of the UGATE signal. For each action, there is a built-in precedent blanking delay following detection of the high-to-low transition 411 of the LGATE signal 410.

[024] The first case (Case I), shown by signal trace 420, corresponds to the polarity of the voltage at the PHASE node 5 going negative subsequent to the LGATE node transitioning from high-to-low at 411, referenced above. For this purpose, in response to the LGATE voltage going low at 411, the voltage at the PHASE node 5 is monitored to determine whether it has reached a prescribed negative polarity voltage (e.g., -0.4 V). In particular, following a (7 ns) blanking delay 410-D, if the phase voltage at the PHASE node 5 drops below the -0.4 V threshold as shown at 421, combinational logic 60 triggers a low-to-high to transition on the UGATE, which causes the phase node voltage to go high at 422.

[025] The second case (Case II) shown by signal trace 430 is associated with a reverse current condition, and corresponds to the polarity of the voltage at the PHASE node going positive subsequent to the LGATE node transitioning from high-to-low 411. For this purpose, if Case I is not observed, namely, if the -0.4 V threshold 421 is not reached following the high-to-low transition

of the LGATE voltage, combinational logic 60 looks to see whether a prescribed positive threshold (e.g., +0.6 V) has been reached. If so, as shown by threshold 431, combinational logic 60 will trigger a low-to-high transition of the UGATE signal, which causes the phase node voltage to go high, as shown at 432.

[026] The third case (Case III), shown by signal trace 440, and associated with a no load condition, corresponds to the elapse of a prescribed time-out without either of the positive and negative polarity thresholds having been reached at the phase node 5. Namely, if neither the -0.4 V and +0.6 V thresholds described above, is observed at the phase node 5 within a prescribed time out window 440-TO (e.g., 50 ns) after the high-to-low transition 411 in the LGATE signal 410, the combination logic 60 triggers a low-to-high transition of the UGATE signal so that the voltage at the phase node 5 goes high as shown at 441.

[027] From a comparison of the LGATE turn-off transition 411 with the respective UGATE turn-on transitions represented by the phase node voltage traces 422, 432 and 441, it can seen that there is no overlap between the terminal end of the conduction interval for LFET 4 and the initial portion of the conduction interval for the UFET 3. Therefore, there is no simultaneous conduction of these two FETS between the time of turn-off of the LFET and the time of turn-on of the UFET 3 in response to a low-to-high transition in the PWM signal.

[028] The timing diagrams of Figures 5A-5C detail the controlled turn-off of UFET 3 and the subsequent turn-on of LFET 4, after a high-to-low transition 501 in the PWM signal 500. In particular, as shown by broken lines 502, turn off of the UGATE drive to UFET 3 is initiated at 511 by the high-to-low transition 501 in the PWM waveform of Figure 5A. Thereafter the PHASE node and UGATE node are monitored by associated threshold circuits 140 -160 within the dead time controller 100. Specifically, in response to the UGATE voltage dropping to a voltage level that is a prescribed value above the phase voltage (e.g., on the order of 1.75 V above the PHASE voltage (112V)), as shown at 511, a prescribed time out (e.g., 10 ns) is triggered, as shown by broken lines 521, whereupon the LGATE signal 520 is transitioned from low-to-high at 522, turning on the LFET 4.

[029] Alternatively, if the level of the PHASE node voltage 530 reaches a predetermined threshold (e.g., on the order of 0.8 V) as shown at 531, the low-to-high transition of the LGATE voltage is initiated, as shown at 522. As is the case a for a low-to-high transition of the PWM signal, from a comparison of the LGATE turn-on transition 522 with the UGATE turn-off transition 511, it can seen that there is no overlap between the terminal end of the conduction interval for the UFET 3 and the initial portion of the conduction interval for the LFET 4, so that simultaneous conduction of the two FETS between turn-off of the UFET 3 and turn-on of the

LFET 4 cannot occur in response to a high-to-low transition in the PWM signal.

[030] While we have shown and described an embodiment in accordance with the present invention, it is to be understood that the same is not limited thereto but is susceptible to numerous changes and modifications as known to a person skilled in the art. We therefore do not wish to be limited to the details shown and described herein, but intend to cover all such changes and modifications as are obvious to one of ordinary skill in the art.